

9 wherein the source region forms a p-n junction in the substrate, a distance of the  
10 source p-n junction from the sidewall being approximately equal to the distance of the extension  
11 of the source contact region from the surface.

Please amend claim 3 as follows:

1 3. (Once Amended) The trench transistor of claim 2 wherein the degree of  
2 overlap is controlled during the manufacture of the transistor so as to provide a predetermined  
3 gate-to-source capacitance.

Please cancel claims 4-6.

Please amend claim 7 as follows.

1 4 7. (Once Amended) The trench transistor of claim 1 wherein both the  
2 distance of the source p-n junction from the sidewall and the distance of the extension of the  
3 source contact region from the surface is less than or equal to about 0.15 microns.

Please amend claim 9 as follows:

1 6 8. (Once Amended) The trench transistor of claim 1 further comprising a  
2 heavy body, the heavy body extending into the inner corner formed by the source region and  
3 the source contact region.

Please add new claims 17-25 as follows.

1 17. (New) A trench transistor comprising:  
2 a substrate;  
3 an epitaxial semiconductor layer of a first conductivity type covering the  
4 substrate;  
5 a semiconductor region of a second conductivity type, opposite that of the first  
6 conductivity type, covering the epitaxial layer;  
7 at least two trenches extending from a surface of the semiconductor region,  
8 through the semiconductor region and partially into the epitaxial semiconductor layer, each  
9 trench defined by sidewalls;  
10 a gate dielectric lining the sidewalls; and  
11 a source region extending from the surface into the semiconductor region  
12 along the sidewalls, the source region having a tapered portion starting from a first depth

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13 from the surface and extending toward the sidewalls to a second depth where the source  
14 region terminates.

1 18. (New) The trench transistor of claim 17, further comprising:  
2 a conductive gate material partially filling the gate-dielectric-lined trenches.

1 19. (New) The trench transistor of claim 18, wherein a depth of the gate  
2 material, measured from the surface of the semiconductor region relative to the second depth  
3 of the source region, is controlled during the manufacture of the trench transistor so as to  
4 provide a predetermined gate-to-source capacitance.

1 20. (New) The trench transistor of claim 17, further comprising:  
2 a heavy body of the second conductivity type extending into the  
3 semiconductor region between trenches, the heavy body having a doping concentration that is  
4 greater than a doping concentration of the semiconductor region.

1 21. (New) The trench transistor of claim 20, further comprising:  
2 a source contact region in contact with the source region, positioned between  
3 trenches and extending less than or equal to about 0.15 microns deep from the surface into  
4 the heavy body.

1 22. (New) The trench transistor of claim 21 wherein the source contact  
2 region forms an inner corner with the source region.

1 23. (New) The trench transistor of claim 22 wherein the heavy body  
2 extends into the inner corner.

1 24. (New) The trench transistor of claim 17 wherein the tapered portion  
2 has a doping concentration that is less than a doping concentration of the remaining portion  
3 of the source region along the sidewalls.

1 25. (New) The trench transistor of claim 17 wherein a doping concentration of  
2 the source region along sidewalls is greater than a doping concentration of the source region near  
3 the surface.

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